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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,232	08/24/2001	William Joseph Armstrong	IBM / 182	4082

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EXAMINER

PROCTOR, JASON SCOTT

ART UNIT	PAPER NUMBER
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2123

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/939,232

Applicant(s)

ARMSTRONG ET AL.

Examiner

Jason Proctor

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 June 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

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DETAILED ACTION

Claims 1-21 are currently pending in the application. Claims 1, 11 and 19 have been amended by RCE submitted on 8 June 2005. Claims 1-21 have been rejected.

Response to Rejections under 35 U.S.C. § 102

Claims 1-21 were rejected under 35 U.S.C. § 102(b) as being anticipated by US Patent No. 5,872,963 to Bitar et al. (Bitar). In light of Applicants' amendments and arguments, particularly that Bitar fails to disclose "a hypervisor configured to assign and dispatch the CPU to the virtual processors" as recited by independent claims 1, 11 and 19, these rejections have been withdrawn.

Applicants' response states:

During the interview, the Examiner suggested emphasizing the role of a "hypervisor" in the claims and indicated that amendments to that effect would patentably distinguish the claims from the prior art.

The Examiner wishes to clarify that this amendment has patentably distinguished the claims from the prior art relied upon in the previous rejection and has provoked further search of the prior art. A statement to this effect is found in the Interview Summary from 19 April 2005.

Claim Rejections - 35 USC § 101

35 U.S.C. § 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

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1. Claims 19-21 are rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter. The current practice regarding the use of terms such as “signal bearing medium” and “computer-readable medium” is that they are statutory if the specification does not define these terms as including intangible media, such as transmission waves or electrical signals. The specification in this application defines “signal bearing media” as including “transmission type media such as digital and analog communication links”. Therefore claims 19-21, which recite a program product on a signal bearing medium, are nonstatutory. The Examiner respectfully suggests amending claim 19 to read “a tangible signal bearing medium” to limit the claimed invention to statutory embodiments. The limitations of claim 20 may face additional complications in that claim 20 appears to recite, in effect, that the program product is either tangible or intangible. As set forth above, only the tangible embodiments are statutory.

To expedite a complete examination of the instant application the claims rejected under 35 U.S.C. § 101 (nonstatutory) above are further rejected as set forth below in anticipation of applicant amending these claims to place them within the four statutory categories of invention.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
 2. Ascertaining the differences between the prior art and the claims at issue.
 3. Resolving the level of ordinary skill in the pertinent art.
 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
2. Claims 1-21 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 5,404,563 to Green et al. (Green) in view of US Patent No. 5,872,963 to Bitar et al. (Bitar).

Green provides background knowledge of what is known in the art regarding a hypervisor on a logically partitioned computer system (column 1, lines 10-54). In particular, Green teaches, "The hypervisor 112 schedules, or allocates, the physical hardware components 104 to the logical partitions 114. For example, during a particular time-slice, the hypervisor 112 may allocate the physical CPU 106A to operate with the logical partition 114A. Specifically, the hypervisor 112 may dispatch the logical CPU 116B on the physical CPU 106A." (column 1, lines 33-43). Green does not disclose or teach the claimed scheduling scheme.

Bitar discloses the claimed scheduling scheme as a method for context switching between execution entities (abstract) wherein the execution entities may be virtual processors (column 1, lines 34-40; column 1, lines 55-63) but are equivalently described by Bitar as threads ["*A virtual processor may be a process, [...] a kernel thread, [...] or some other abstraction.*" (column 1,

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lines 34-40); *“This abstraction, a virtual processor, is scheduled by the operating system scheduler for execution on available physical processors.”* (column 1, lines 55-63)].

Bitar’s method of switching between entities comprises a yielding virtual processor [*“threads which have finished their work”*, (column 10, line 48 – column 11, line 10)] which designates a target virtual processor [*“can transfer control of their respective processors to the preempted threads, thus resuming them.”* (column 10, line 48 – column 11, line 10); *“thread B can transfer its processor to thread A, thus resuming thread A”* (column 11, lines 33-41)] and switching-in the target virtual processor for execution by the CPU in response to the requested yield [*“resuming thread them”*; *“resuming thread A”*; *supra*].

It would have been obvious to a person of ordinary skill in the art at the time of Applicants’ invention to combine the teachings of Bitar regarding designating a target virtual processor by a yielding virtual processor on a logically partitioned computer system using a hypervisor because Green expressly teaches that the hypervisor schedules virtual processors and Bitar teaches an improved scheduling algorithm for dealing with situations such as spin locks (as in column 11, lines 33-41). The combination could be formed by implementing the processor control transfer method taught by Bitar in the logically partitioned hypervisor system of Green.

The rejections of claims 2-21 incorporate the rejection and combination formed above in regard to claim 1.

Regarding claim 2, Bitar et al. teaches a method of context switching wherein the target virtual processor requires access to the CPU, wherein the yielding virtual processor controls the CPU (column 10, line 48 – column 11, line 10; column 11, lines 33-41).

Regarding claim 3, Bitar et al. teaches a method of context switching comprising generating a yield command from the virtual processor, wherein the yield command includes pointer and status information regarding the target virtual processor (column 10, lines 9-33).

Regarding claim 4, Bitar et al. teaches a method of context switching comprising assigning status information to the target virtual processor (column 10, lines 9-33).

Regarding claim 5, Bitar et al. teaches a method of context switching comprising assigning a target count to the target virtual processor (column 10, lines 9-33). The preempt bit vector holds a value of 0 for a thread that has its resource requirements fulfilled and holds a value of 1 for a thread that has been preempted and requires resources to continue.

Regarding claim 6, Bitar et al. teaches a method of context switching comprising comparing the target count to a presented count conveyed in the yield request (column 10, lines 9-33; column 13, line 53 – column 14, line 24; column 16, lines 29-44).

Regarding claim 7, Bitar et al. teaches a method of context switching comprising aborting the yield in response to a yield-to-active command. If the processor is not needed, it will be reallocated to another process (column 16, lines 29-44).

Regarding claim 8, Bitar et al. teaches a method of context switching comprising designating the yielding virtual processor as waiting for the target virtual processor (column 10, line 48 – column 11, line 10; column 11, lines 33-41; column 16, lines 29-44).

Regarding claim 9, Bitar et al. teaches a method of context switching comprising designating the target virtual processor as having a yielding processor waiting for the target virtual processor (column 13, line 53 – column 14, line 24; column 16, lines 29-44).

Regarding claim 10, Bitar et al. teaches a method of context switching comprising storing the state of the yielding virtual processor (column 10, lines 9-33; column 13, lines 53-60).

Claims 11-18 are directed toward an apparatus comprising a computer system and a computer program to execute the method of claims 1-3, and 5-9. As the invention of Bitar et al. is a computer system and program (abstract), claims 11-18 are rejected for reasons similar to those given for claims 1-3, and 5-9 above.

Claims 19 and 20 are directed toward a program product and signal bearing medium bearing a computer program which executes the method of claim 1. As the invention of Bitar et

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al. can be realized with a computer program, whether transmitted via a network or stored locally (abstract; column 17, lines 20-27; column 20, line 49 – column 21, line 10), claims 19 and 20 are rejected for reasons similar to those given for claim 1 above.

Regarding claim 21, Bitar teaches a user-level scheduler which includes a queue (schedule) used to schedule ready-to-run threads (column 8, lines 21-31). It is inherent that a user-level scheduler is a thread, therefore a virtual processor.

Conclusion

Art considered pertinent by the examiner but not applied has been cited on form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.


Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR)

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system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
Art Unit 2123

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Paul L. Rodriguez 8/31/05
Primary Examiner
Art Unit 2125